REMARKS

Reconsideration and allowance of the above-referenced application are respectfully requested. Claims 1-9 are unchanged, claims 10-13 are added, and claims 1-13 are pending in the application.

The objection to the drawings is acknowledged. It is believed the drawings as amended are in proper form.

Claims 1-9 stand rejected under 35 USC §102(b) in view of U.S. Patent No. 6,097,767 to Lo. This rejection is respectfully traversed.

Each of the independent claims 1 and 6 specify an arrangement for supplying equalizer settings to a digital ***feedforward*** equalizer. In particular, each of the independent claims specify: (1) supplying a prescribed initial set of equalizer settings to the digital feedforward equalizer, (2) comparing the equalized signal samples relative to a prescribed ***equalization*** threshold, and (3) ***selectively changing*** the supplied equalizer settings, based on the comparing step, ***until*** *the equalized signal samples reach the* ***prescribed equalization threshold***.

As described on page 3, lines 14-23 of the specification:

> Supplying the prescribed initial set of equalizer settings enables the digital feedforward equalizer to begin equalizing the retrieved signal samples, *regardless of whether other portions of the physical layer transceiver, such as the slicer, timing recovery unit, etc., have been able to begin recovery of information from the retrieved signal samples.* Moreover, ***the selective changing of the supplied equalizer settings until the equalized signal samples reach the prescribed equalization threshold*** enables the independent initialization of the digital feedforward equalizer, enabling other portions such as the timing recovery unit to begin recovery of information concurrent with the independent initialization of the digital feedforward equalizer, improving the physical layer transceiver efficiency in establishing timing recovery and intersymbol interference equalization for symbol recovery.

Hence, use of a digital feedforward equalizer enables rapid convergence based on the independent initialization by selectively changing the supplied equalizer settings until the prescribed equalization is reached, while minimizing the introduction of instability due to unsettled data (see, e.g., page 5, line 31 to page 6, line 3 of the specification).

The use of a digital ***feedforward*** equalizer, plus the ***selective changing*** of the supplied

equalizer settings ***until the equalized signal samples reach the prescribed equalization threshold***, is neither disclosed nor suggested in the applied prior art.

Lo describes an equalization technique that relies on a closed loop system using a ***phase locked loop*** (PLL) (see, e.g., Abstract at lines 10-13; col. 2, lines 30-34; col. 3, lines 16-24). In particular, Lo relies on a PLL 34 to identify a *timing correlation* of an edge of an equalized signal relative to a recovered clock signal (RCLK):

> The digital phase locked loop 34, in response to receiving the equalized signal from the equalizer 32, generates a recovered clock signal (RCLK) and recovered data signal (RDATA) based upon ***sampling the equalized signal with the recovered clock signal.*** The digital PLL 34 also generates ***a correlation result (SEG) that specifies a timing correlation of an edge of the equalized signal relative to the recovered clock signal (RCLK).*** Specifically, FIG. 3 is a diagram that illustrates sampling techniques used by the digital PLL 34 to recover the transmitted data. As shown in FIG. 3, the digital PLL 34 correlates the recovered clock (RCLK) with the equalized signal (ES). Ideally, the bits in the equalized signal (ES) are recovered by sampling at the center of each bit, indicated by the arrow 38. As shown in FIG. 3, the rising edge of the recovered clock (RCLK) coincides with the optimal sampling points 38. Jitter in the equalized signal (ES) causes an edge 40 of the equalized signal to be shifted by an amount (J) such that the ideal signal edge 40 may be shifted to edges 40a or 40b by an amount J.
>
> (Col. 4, lines 6-24).

Lo further describes that the optimum equalizer setting is chosen based on determining the relative edge distribution for each equalizer setting, and identifying the corresponding relative edge distribution that demonstrates the ***minimum distribution of jitter*** (i.e., based resembling the distribution curve 46 of Fig. 4A, see col. 4, lines 47-50):

> According to the disclosed embodiment, the equalizer controller 36 counts the number of transitions occurring in any of the four segments 48, 50, 52, 54 [of Fig. 4A or 4B], and selects as an optimal equalizer setting the one predetermined equalizer setting that results in the minimum number of transitions occurring in the outer regions 48 and 54. Specifically, the digital PLL 34, in response to detecting an edge transition 40 relative to a clock pulse edge 44, outputs a segment signal (SEG) as a digital code that identifies the distribution range 48, 50, 52, or 54 that corresponds to the timing correlation between the detected edge 40 of the equalized signal (ES) and the edge 44 of the recovered clock signal (RCLK).

(Col. 4, line 61 to col. 5, line 5).

Consequently, Lo requires that each and every equalizer setting be evaluated to determine the corresponding edge distribution to identify the ***minimum jitter*** :

> FIG. 5 is a block diagram illustrating a state machine 70 in the equalizer controller 36 for determining the normalized distribution result for each of the predetermined equalizer settings, and selecting the optimum equalizer setting according to an embodiment of the present invention.
>
> (Col. 5, lines 23-26).
>
> [T]he equalizer controller 36 moves to the try next setting state 80 if the selected equalizer setting (eq.sub.-- setting) is less than the maximum equalizer setting (MAX), ***indicating that additional equalizer settings still need to be tested.***
>
> (Col. 6, lines 61-65).

As apparent from the foregoing, Lo provides no disclosure whatsoever of the claimed "digital ***feedforward*** equalizer", as claimed. Nor does Lo provide any suggestion of any digital feedforward equalizer, since Lo relies on using a PLL in a closed loop system to determine the minimum jitter. For this reason alone, the rejection should be withdrawn because it fails to demonstrate that Lo discloses each and every element of the claim. See MPEP 2131. "The identical invention must be shown in as complete detail as is contained in the ... claim." Richardson v. Suzuki Motor Co., 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989). "Anticipation cannot be predicated on teachings in the reference which are vague or based on conjecture." Studiengesellschaft Kohle mbH v. Dart Industries, Inc., 549 F. Supp. 716, 216 USPQ 381 (D. Del. 1982), aff'd., 726 F.2d 724, 220 USPQ 841 (Fed. Cir. 1984).

Further, as demonstrated above, Lo does not disclose or suggest the claimed "***selectively*** *changing* the supplied equalizer settings, based on the comparing step, ***until the equalized signal samples reach the prescribed equalization threshold***." Rather, Lo requires each and every equalizer setting to be evaluated to determine the minimum jitter, and hence describes ***necessarily*** changing the supplied equalizer settings. Claims 1 and 6, however, specify

"***selectively*** changing", thereby permitting the possibility that the claimed prescribed initial set of equalizer settings may be used, ***without further modification***, based on the prescribed initial set generating equalized signal samples that reach the prescribed equalization threshold. For this reason alone the §102 rejection should be withdrawn.

Applicant traverses the reference to column 6, lines 1-4 as teaching the claimed "prescribed equalization threshold" -- the cited portion describes a signal detection signal that identifies whether a cable is connected to the receiver:

> [T]he equalizer 32 also outputs a reset signal and a detection signal (SIG_DET), which may be used by the equalizer 36 ***to detect an initialization condition*** in the equalizer controller 32, for example a reset state ***or a disconnect state***.
>
> (Col. 4, lines 1-5).
>
> As shown in FIG. 5, the state machine includes a link down state 72, executed by the equalizer controller 36 in response to reception of either a reset signal or ***deassertion of the signal detect signal (SIG_DET), indicating no signal is present on the medium 14***.
>
> (Col. 5, lines 33-37).
>
> The equalizer controller 36 remains the link down state 72 until reception of the detection signal (SIG_DET). The detection signal SEG_DET [sic] is a logical signal output by the equalizer 32 that indicates that signal transitions are occurring above a defined threshold, ***for example when a cable is connected to the receiver 30***.
>
> (Col. 5, line 66 to col. 6, line 4).

Hence, the "threshold" in Lo refers to a basic signal threshold to indicate that the a cable is connected to the receiver, and not the claimed "prescribed ***equalization*** threshold". Anticipation cannot be established based on a piecemeal application of the reference, where the Examiner picks and chooses isolated features of the reference in an attempt to synthesize the claimed invention. "Anticipation requires the presence in a single prior art reference disclosure of each and every element of the claimed invention, arranged as in the claim." *Lindemann Maschinenfabrik GmbH v. American Hoist & Derrick Co.*, 221 USPQ 481, 485 (Fed. Cir. 1984).

Hence, it is not sufficient that a single prior art reference discloses each element that is claimed, but the reference also must disclose that the elements are arranged as in the claims under review. *In re Bond*, 15 USPQ2d 1566, 1567 (Fed. Cir. 1990) (citing *Lindemann Maschinenfabrik GmbH*).

For these and other reasons, the §102 rejection of independent claims 1 and 6 should be withdrawn.

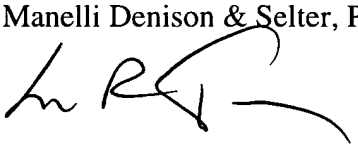
The rejection of claims 4-5 and 9 is further traversed. Lo provides no reference whatsoever to any "absolute value", let alone the claimed location where a statistically substantial number of the data values ***representing a symbol absolute value of "1"*** should occur for an equalized signal. As described above, Lo relies on identifying timing relationships between a equalized signal edge 40 and an edge 44 of the recovered clock. Column 6 of Lo describes identifying whether the timing relationship for each signal edge 40 falls within one of the ***distribution regions*** 48, 50, 52, 54, used to identify ***jitter***.

For these and other reasons, the §102 rejection should be withdrawn.

In view of the above, it is believed this application is and condition for allowance, and such a Notice is respectfully solicited.

To the extent necessary, Applicant petitions for an extension of time under 37 C.F.R. 1.136. Please charge any shortage in fees due in connection with the filing of this paper, including any missing or insufficient fees under 37 C.F.R. 1.17(a), to Deposit Account No. 50-0687, under Order No. 95-525, and please credit any excess fees to such deposit account.

Respectfully submitted,
Manelli Denison & Selter, PLLC



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Date: June 30, 2005

AMENDMENTS TO THE DRAWINGS

The attached sheets of drawings include changes to Figs. 1, 2, and 3 and replace the original sheets including Figs. 1, 2, and 3.

In Fig. 1, a box has been added to indicate that reference numeral 20 identifies the decision feedback equalizer circuit comprising elements 26, 28, 30 (see page 5, lines 28-29 of the specification).

In Fig. 2, a box has been added to indicate that reference numeral 46 identifies the counter circuit comprising elements 54, 56, 58 (see page 7, line 12 of the specification), and the arrow for reference numeral 34 has been corrected.

In Fig. 3, the decision labels "Yes" and "No" have been added with respect to step 90.

Attachment: 3 Replacement Sheets

3 Annotated Sheets Showing Changes

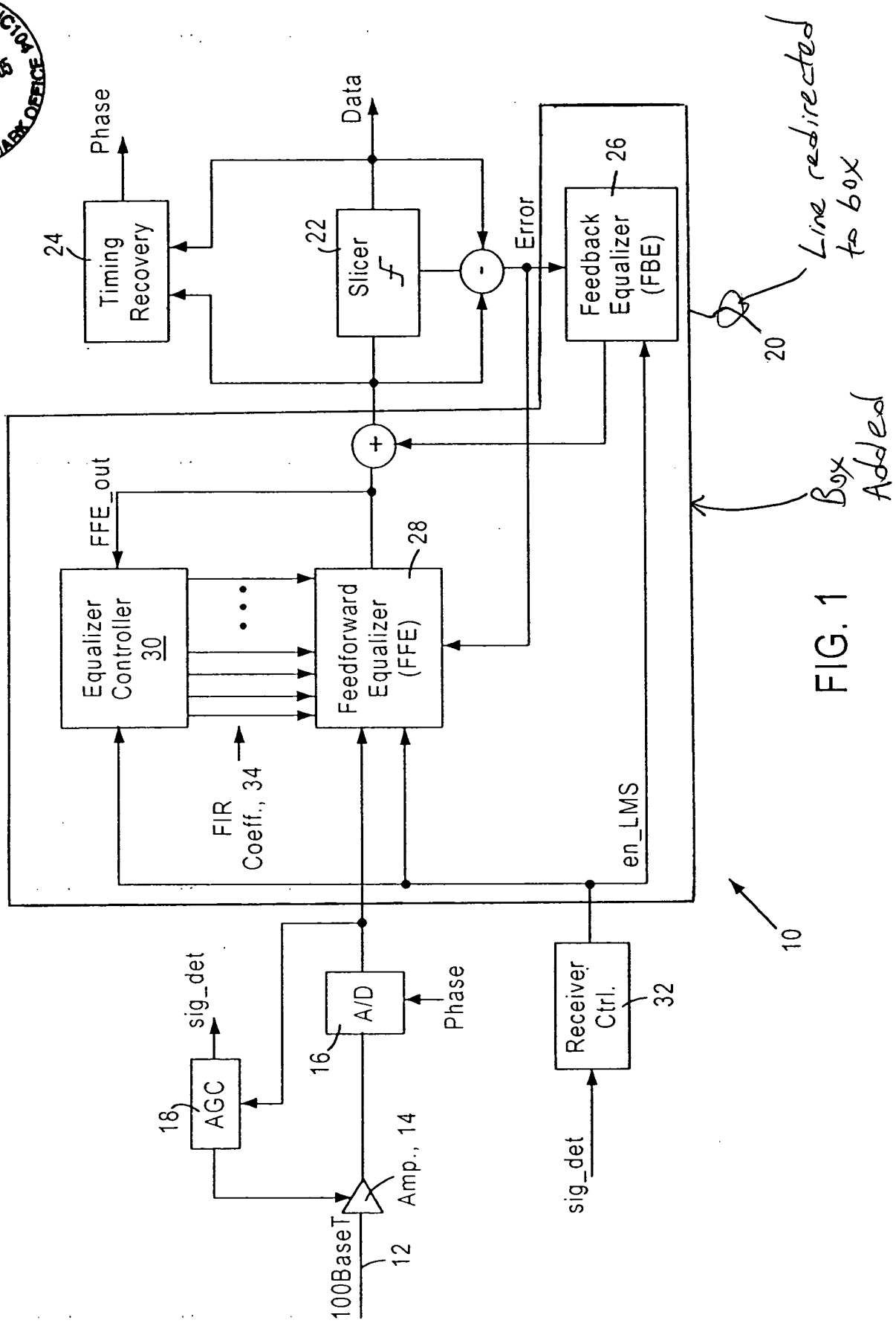

FIG. 1

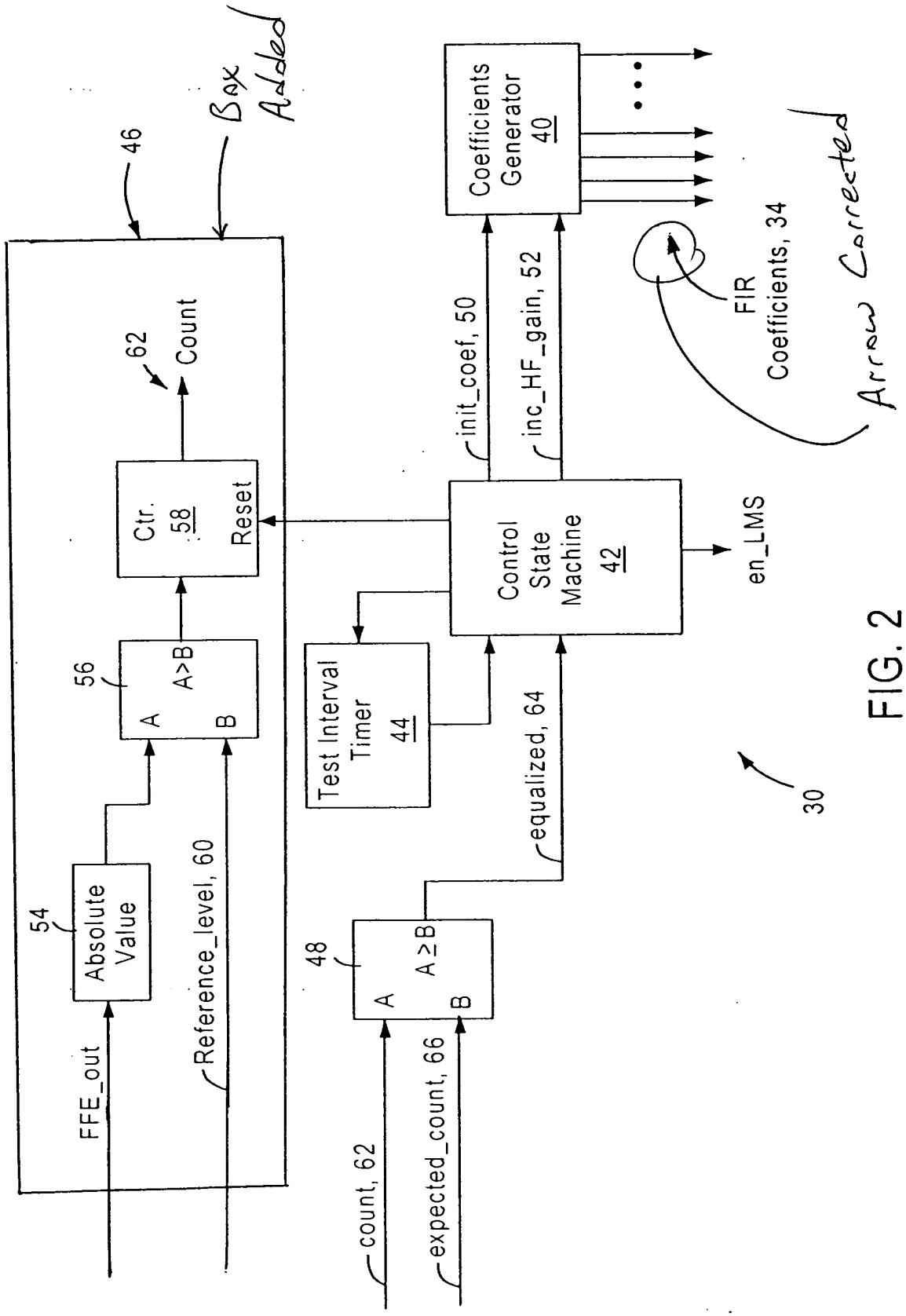
Box Added
46
Coefficients Generator 40
FIR Coefficients, 34
Arrow Corrected
init_coef, 50
inc_HF_gain, 52
62
Count
Ctr. 58
Reset
Control State Machine 42
en_LMS
56
A>B
A
B
Test Interval Timer 44
equalized, 64
54
Absolute Value
48
A≥B
A
B
FFE_out
Reference_level, 60
count, 62
expected_count, 66
30

FIG. 2

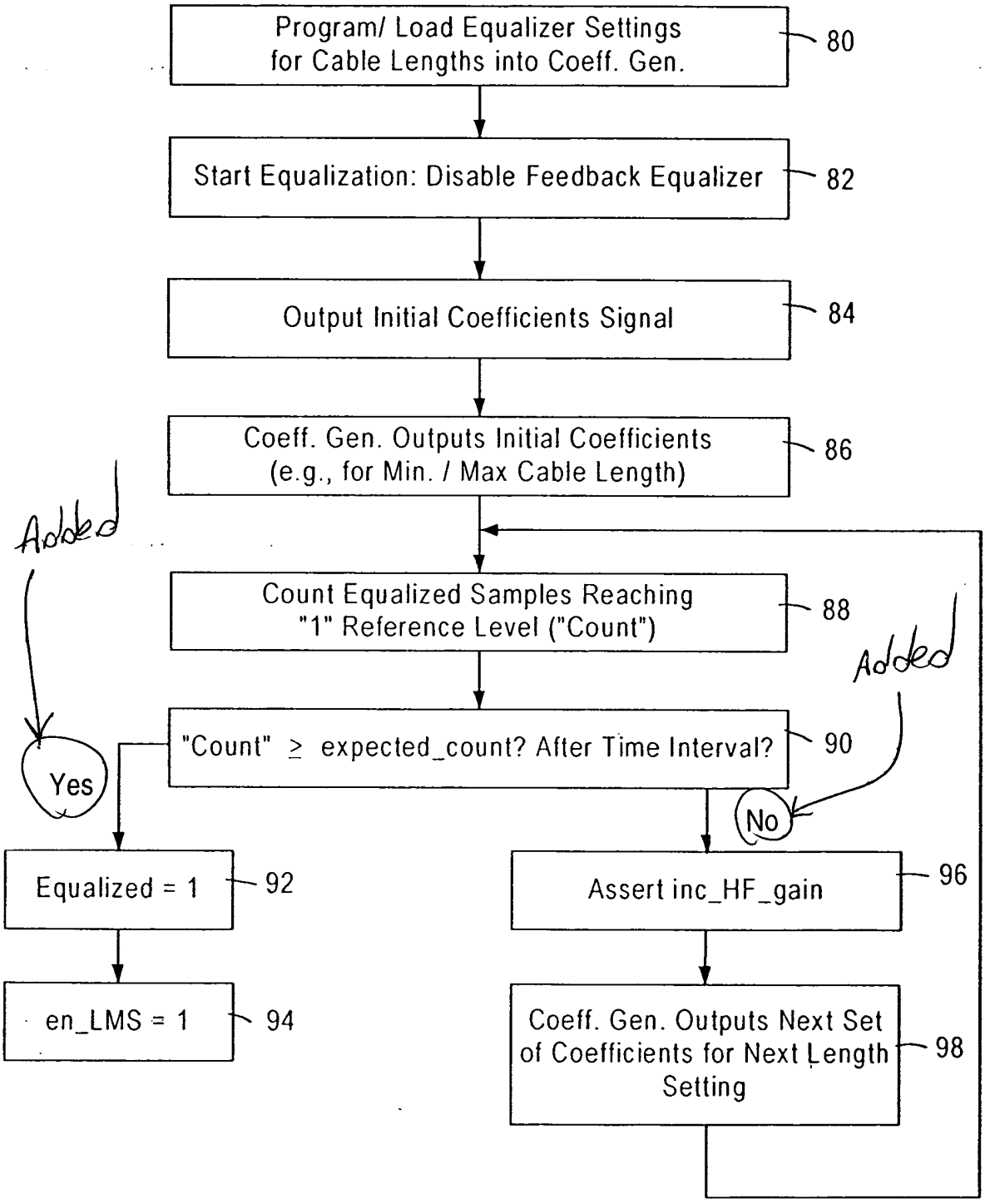
Program/ Load Equalizer Settings for Cable Lengths into Coeff. Gen.
80
Start Equalization: Disable Feedback Equalizer
82
Output Initial Coefficients Signal
84
Coeff. Gen. Outputs Initial Coefficients (e.g., for Min. / Max Cable Length)
86
Added
Count Equalized Samples Reaching "1" Reference Level ("Count")
88
Added
"Count" ≥ expected_count? After Time Interval?
90
Yes
No
Equalized = 1
92
Assert inc_HF_gain
96
en_LMS = 1
94
Coeff. Gen. Outputs Next Set of Coefficients for Next Length Setting
98

FIG. 3